Stratix V GXのPCI Express x8 Gen3 ボード。デバイスドライバを含むPCIe ホストI/FとDDR3 メモリI/Fが容易に使えるように整備されたGiDELのProceVは、拡張バスでアプリ固有の機能（たとえばMIPI PHY）を追加するだけで様々に使える実戦型FPGAボード。

think SPEED think GiDEL™

# ProceV™

PRELIMINARY PRODUCT BRIEF
December 2012

# PCIe x8 (Gen 3) FPGA Computation Accelerator

## Key Features

- Altera Stratix V GX (A3, A7, AB)/GS (D5, D8) FPGAs
- 8-lane PCI Express Gen3 (PCIe x8) host interface
- Dynamically reconfigurable FPGA
- Reconfigurable transceivers supporting multiple protocols and data rates
- Up to 3,926 18×18 Variable Precision Multipliers
- 1 CXP connector cage suitable for 100 Gigabit Ethernet (100GBASE-CR10, 100GBASE-SR10), 3×40 Gigabit Ethernet, or single Infiniband 12×QDR link
- 2 SFP+ cage suitable for 10 Gigabit Ethernet and Optical Transport Network
- RJ45 port suitable for 1000MBase-T and 100MBase-TX
- 2× High-Speed Inter-Board connectors (up to 12×14.1Gb/s full duplex GPIO) for board to board and proprietary daughterboards connectivity
- 12 general purpose LVTTL External IOs
- External clock input via an SMA connector
- Four level memory structure (**16+ GB**).
  Typical sustain throughput of **8000 GB/s** for internal memories and **25**+ **GB/s** for on-board memory as follows:
  - Up to 2640 M20K (20K-bit) SRAM blocks (52 Mb) with a typical throughput of **8,000 GB/s** at 300 MHz
  - Up to 17,960 Enhanced MLAB (640-bit) SRAM blocks (8 Mb)
  - 2 ×DDR3 ECC SODIMMs Banks with up to **a** total of 16 GB at a maximum sustain throughput of **19.2 GB/s**
  - Optional: 2× 144Mb SRAM memories (up to **450Mhz**) at a sustain throughput of **6.4 GB/s**
- Support for a single PSDB type 1 daughter board used for a GiDEL's off-the-shelf or user add-on Interface
- Stand-alone mode
- Typical system frequencies: 150-450 MHz
- Flexible clocking system
- Volatile and non-volatile design security
- Supported by GiDEL's ***ProcDeveloper's Kit***
- Low power technology

## Benefits

- Leading edge performance
- Unique development tools reducing the development cycle and simplifying maintenance and upgrade tasks.
- Maintainability, Reliability and long life cycle


## Overview

The ProceV system is based on Altera's newest generation Startix V FPGA device. The ProceV provides massive capacity (up to 952K LEs), and high memory and I/O performance. In addition to 8-Lane PCIe gen 3, twenty six 12.5/14.1 Gb/s transceivers provide external IOs of up to 366 Gb/s (full duplex). The combination of high-speed direct communication to the FPGA via PCIe, CXP, SFP+, and General Purpose high-speed transceivers makes the ProceV ideal for low-latency, high performance networking and HPC applications. Powerful memory scheme, composed of embedded memory with 8 TB/s throughput, 16 GB ECC DDR III and optional 288 Mb DDR II SRAM, enables high bandwidth computation and networking, and unique flexibility to achieve diverse algorithm architectures. Using an external clock, a GiDEL or user dedicated add-on daughter boards, the FPGA device can directly interface with standard protocols such as HDMI, SDI and Camera Link as well as with user's propriety IO systems. Eight-lane PCIe Gen. 3 interface allows for strong co-processing between a standard PC operating system and an FPGA based accelerator. The ProceV system conjoined with GiDEL's ProcDeveloper's Kit maximizes system performance while significantly improving development productivity. Based on this powerful development suite, for over 15 years GiDEL has consistently been able to meet unique costumer requirements while allowing for flexibility to accommodate long-term product evolution.


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## Target Application Examples

- ✓ Trading
- ✓ Life science Applications
- ✓ Surveillance, Machine Vision and Imaging
- ✓ ASIC and SoC Prototyping
- ✓ DSP (Digital Signal Processing) and HPRC (High Performance Reconfigurable Computing)
- ✓ High-speed low latency networking and network analysis
- ✓ High performance acquisition systems

## Development Environment

The ProcDeveloper's Kit, GiDEL's intuitive design and debug environment, facilitates design development effort on the ProceV system. The kit contains ***ProcWizard***™, ***ProcMultiPort***™ and other IPs, ***Quartus II***, ***USBBlaster***, and optional ***ProcHILs***™ and ***TotalHistory***™.

The ***ProcHILs***, based on an intuitive interface, enables to use ***Simulink*** as a design entry tool to achieve full system performance while the algorithm developer does not require any knowledge of HDL language. In addition, the ProcHILs using Hardware in the Loop (HIL) methodology enables to significantly accelerate Simulink simulation by taking advantage of the FPGA's high performance capabilities.

Other high-level design entry options, such as C++, are available via GiDEL's partners.

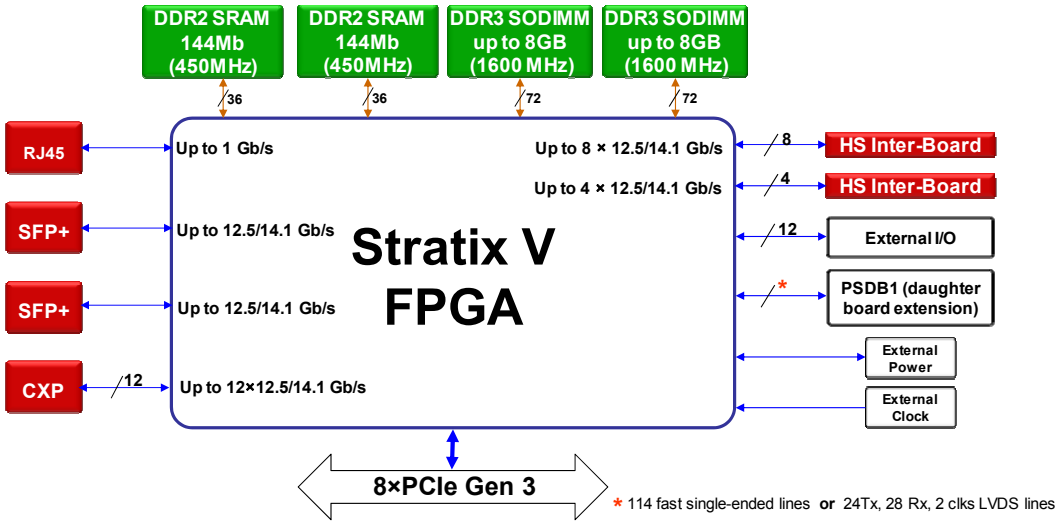
The ***ProcWizard*** performs hardware initialization and automatically generates the following:

- Top-level designs, interface modules/entities and on-board memory controllers for application use.
- Device constraints (e.g., timing, pin-outs and drive strength).
- C++ class(es) application driver(s) enable simultaneous accesses of multiple applications, each to its' dedicated section of the Proc board.
- Interface documentation in HTML or MS Word.

The ***ProcMultiPort*** IP and other GiDEL memory control IPs, such as the ***MegaFIFO*** IP, provide simple access to the on-board DRAM. The ProcMultiPort splits the memory into several logical memories, each accessible simultaneously by multiple ports. As a result, the on-board memory is mapped according to the desired algorithm and not vice versa. The main benefits are:

- Simplification of design and enhanced system performance.
- Design compatibility and migration amongst legacy and future GiDEL Proc boards.
- Replaces the need for inventory of special memories by using standard memory and IP.

GiDEL's ***TotalHistory*** provides virtually unlimited visibility depth to internal signals, taking advantage of unused on-board memory. TotalHistory requires no additional hardware and may work at your customers' site to support remote debugging.

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